Ordering number : ENN6067A

Monolithic Digital IC

LB1923M

Power Brushless Motor Pre-Driver IC for OA Equipment

Overview

The LB1923M is a pre-driver IC that supports direct PWM drive and is appropriate for the power brushless motors used in office automation equipment. A motor drive circuit with the desired output capability (voltage and current characteristics) can be constructed by attaching a driver array at the IC output. The LB1923M includes on chip a speed control circuit that allows the motor speed to be varied using an external clock.

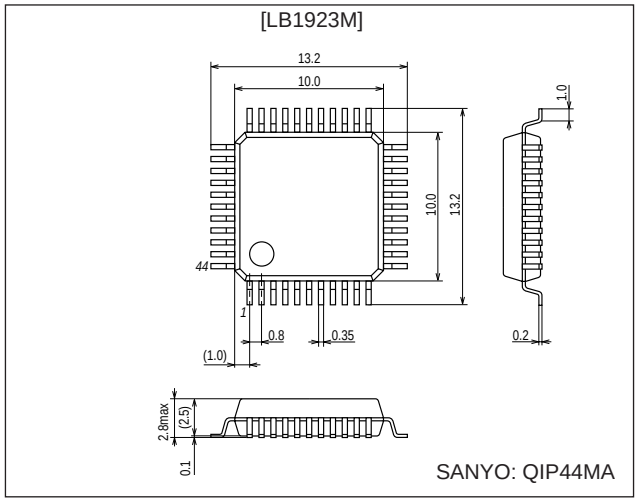
Features

- Direct PWM drive output
- Speed discriminator + PLL speed control circuit
- FG and integrating amplifiers
- Forward/reverse switching circuit
- Braking circuit (short braking)
- Speed lock detection output
- Full complement of on-chip protection circuits, including lock protection, current limiter, and thermal shutdown protection circuits.

Package Dimensions

unit: mm

3148A-QFP44MA



Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		9	V
Maximum input current	I_{REG} max	V_{REG} pin	10	mA
Output current	I_O max	UL, VL, and WL outputs	30	mA
Allowable power dissipation	Pd max		0.9	W
Operating temperature	Topr		–20 to +80	°C
Storage temperature	Tstg		–55 to +150	°C

Allowable Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		4.4 to 7.0	V
Input current range	I_{REG}	V_{REG} pin (7 V)	1 to 5	mA
FG Schmitt output applied voltage	V_{FGS}		0 to 8	V
FG Schmitt output current	I_{FGS}		0 to 5	mA
Lock detection output current	I_{LD}		0 to 20	mA

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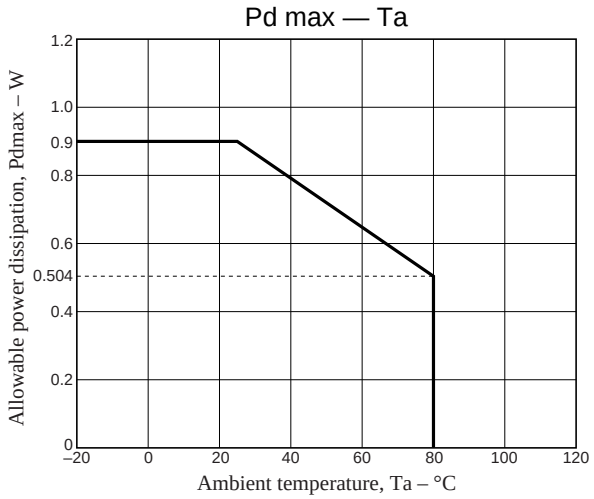
42003AS (OT) / 63099TH (OT) No. 6067-1/17



Electrical Characteristics at Ta = 25°C, V_{CC} = 6.3 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current drain	$I_{CC}1$			42	60	mA
	$I_{CC}2$	In stop mode		10	20	mA
	$I_{CC}3$	V_{CC} = 5 V		38	55	mA
	$I_{CC}4$	V_{CC} = 5 V, In stop mode		8	18	mA
Output saturation voltage	V_O (sat)	UL, VL, WL output, I_O = 20 mA		0.2	0.7	V
Output current	I_O	UH, VH, WH output, V_{OUT} = 1.4 V	–20	–16	–12	mA
Output leakage current	I_O leak	UL, VL, WL output			100	µA
Output off voltage	V_O off	UH, VH, WH output			0.5	V
[Hall Amplifier]						
Input bias current	$I_{HB(HA)}$		–4	–1		µA
Common-mode input voltage range	V_{ICM}		1.5		V_{CC} – 1.5	V
Hall input sensitivity	$\Delta V_{IN(HA)}$		60			mVp-p
Hysteresis	$\Delta V_{IN(HA)}$		17	32	60	mV
Input voltage low → high	V_{SLH}		8	16	30	mV
Input voltage high → low	V_{SHL}		–30	–16	–8	mV
[CR Oscillator]						
Output high-level voltage	$V_{OH(CR)}1$		3.1	3.4	3.7	V
	$V_{OH(CR)}2$	V_{CC} = 5 V	2.4	2.7	3.0	V
Output low-level voltage	$V_{OL(CR)}1$		1.5	1.8	2.1	V
	$V_{OL(CR)}2$	V_{CC} = 5 V	1.1	1.4	1.7	V
Oscillator frequency	$f_{(CR)}$	R = 75 kΩ, C = 1500 pF		19		kHz
Amplitude	$V_{(CR)}1$		1.4	1.6	1.8	Vp-p
	$V_{(CR)}2$	V_{CC} = 5 V	1.1	1.3	1.5	Vp-p
[CROCK Oscillator]						
Output high-level voltage	$V_{OH(RK)}1$		3.2	3.5	3.8	V
	$V_{OH(RK)}2$	V_{CC} = 5 V	2.5	2.8	3.1	V
Output low-level voltage	$V_{OL(RK)}1$		0.8	1.1	1.4	V
	$V_{OL(RK)}2$	V_{CC} = 5 V	0.6	0.9	1.2	V
External capacitor charge current	$I_{CHG}1$		–17	–13	–9	µA
External capacitor discharge current	$I_{CHG}2$		9	13	17	µA
Oscillator frequency	$f_{(RK)}$	C = 0.068 µF		35		Hz
Amplitude	$V_{(RK)}1$		2.2	2.4	2.6	Vp-p
	$V_{(RK)}2$	V_{CC} = 5 V	1.7	1.9	2.1	Vp-p

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[VCO Oscillator]						
Pin C output high-level voltage	$V_{OH(C)}1$		4.1	4.3	4.6	V
	$V_{OH(C)}2$	V_{CC} = 5 V	3.2	3.4	3.6	V
Pin C output low-level voltage	$V_{OL(C)}1$		3.6	3.9	4.1	V
	$V_{OL(C)}2$	V_{CC} = 5 V	2.8	3.0	3.2	V
Oscillator frequency	$f_{(C)}$				1.0	MHz
Amplitude	$V_{(C)}$		0.2	0.4	0.6	Vp-p
[Current Limiter Operation]						
Limiter	V_{RF}		0.47	0.52	0.57	V
[Thermal Shutdown Operation]						
Thermal shutdown operating temperature	TSD	Design target value*	150	180		°C
Hysteresis	ΔTSD	Design target value*		30		°C
[V_{REG} Pin]						
V_{REG} pin voltage	V_{REG}		6.7	7.1	7.4	V
[FG Amplifier]						
Input offset voltage	$V_{IO(FG)}$		–10		+10	mV
Input bias current	$I_{B(FG)}$		–1		+1	μA
Output high-level voltage	$V_{OH(FG)}$		V_{CC} – 1.5	V_{CC} – 1		V
Output low-level voltage	$V_{OL(FG)}$			1	1.5	V
FG input sensitivity		Gain: 100×	3			mV
Schmitt amplitude for the next stage			100	180	250	mV
Operating frequency range					16	kHz
Open-loop gain		$f_{(FG)}$ = 2 kHz	45	51		dB
[FGS Output]						
Output saturation voltage	$V_{O(FGS)}$	$I_{O(FGS)}$ = 2 mA		0.1	0.5	V
Output leakage current	$I_{L(FGS)}$	V_O = V_{CC}			10	μA
[Speed Discriminator Output]						
Output high-level voltage	$V_{OH(D)}$		V_{CC} – 1.0	V_{CC} – 0.7		V
Output low-level voltage	$V_{OL(D)}$			0.4	1.1	V
[Speed Control PLL Output]						
Output high-level voltage	$V_{OH(P)}1$		4.05	4.35	4.65	V
	$V_{OH(P)}2$	V_{CC} = 5 V	3.25	3.55	3.83	V
Output low-level voltage	$V_{OL(P)}1$		1.85	2.15	2.45	V
	$V_{OL(P)}2$	V_{CC} = 5 V	1.25	1.55	1.85	V
[VCO PLL Output]						
Output high-level voltage	$V_{OH(VCO)}$		5.3	5.6		V
Output low-level voltage	$V_{OL(VCO)}$			0.4	11	V
[Lock Detection]						
Output saturation voltage	$V_{OL(LD)}$	I_{LD} = 10 mA		0.1	0.5	V
Output leakage current	$I_{L(LD)}$	V_O = V_{CC}			10	μA
Lock range			–6.25		+6.25	%
[Integrator]						
Input offset voltage	$V_{IO(INT)}$		–10		+10	mV
Input bias current	$I_{B(INT)}$		–0.4		+0.4	μA
Output high-level voltage	$V_{OH(INT)}$		V_{CC} – 1.2	V_{CC} – 0.8		V
Output low-level voltage	$V_{OL(INT)}$			0.8	1.2	V
Open-loop gain			60			dB
Gain-bandwidth product				1.6		MHz
Reference voltage	$V_{B(INT)}$		–5%	V_{CC}/2	5%	V
[Filter Amplifier]						
Input bias current	$I_{B(FIL)}$		–0.4		+0.4	μA
Output high-level voltage	$V_{OH(FIL)}$		V_{CC} – 1.2	V_{CC} – 0.8		V
Output low-level voltage	$V_{OL(FIL)}$			0.8	1.2	V
Reference voltage	$V_{B(FIL)}1$		–5%	2.0	+5%	V
	$V_{B(FIL)}2$	V_{CC} = 5 V	1.5	1.6	1.7	V

Note: * Design target value. These items are not tested.

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Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[S/S Pin]						
Output high-level voltage	$V_{OH(S/S)}$		4.0		V_{CC}	V
Output low-level voltage	$V_{OL(S/S)}$		0		1.5	V
Hysteresis	$\Delta V_{IN(S/S)}1$		0.35	0.45	0.55	V
	$\Delta V_{IN(S/S)}2$	V_{CC} = 5 V	0.24	0.34	0.44	V
Pull-up resistance	$R_{U(S/S)}$		45	63	85	kΩ
[F/R Pin]						
Input high-level voltage	$V_{IH(F/R)}$		4.0		V_{CC}	V
Input low-level voltage	$V_{IL(F/R)}$		0		1.5	V
Hysteresis	$\Delta V_{IN(F/R)}1$		0.35	0.45	0.55	V
	$\Delta V_{IN(F/R)}2$	V_{CC} = 5 V	0.24	0.34	0.44	V
Pull-up resistance	$R_{U(F/R)}$		45	63	85	kΩ
[BR Pin]						
Input high-level voltage	$V_{IH(BR)}$		4.0		V_{CC}	V
Input low-level voltage	$V_{IL(BR)}$		0		1.5	V
Hysteresis	$\Delta V_{IN(BR)}1$		0.35	0.45	0.55	V
	$\Delta V_{IN(BR)}2$	V_{CC} = 5 V	0.24	0.34	0.44	V
Pull-up resistance	$R_{U(BR)}$		45	63	85	kΩ
[CLK Pin]						
Input high-level voltage	$V_{IH(CLK)}$	Design target value*	4.0		V_{CC}	V
Input low-level voltage	$V_{IL(CLK)}$	Design target value*	0		1.5	V
Hysteresis	$\Delta V_{IN(CLK)}1$	Design target value*	0.35	0.45	0.55	V
	$\Delta V_{IN(CLK)}2$	V_{CC} = 5 V, Design target value*	0.24	0.34	0.44	V
Pull-up resistance	$R_{U(CLK)}$		45	63	85	kΩ
Input frequency	$f_{(CLK)}$				16	kHz
[N1 Pin]						
Input high-level voltage	$V_{IH(N1)}$		4.0		V_{CC}	V
Input low-level voltage	$V_{IL(N1)}$		0		1.5	V
Hysteresis	$\Delta V_{IN(N1)}1$		0.35	0.45	0.55	V
	$\Delta V_{IN(N1)}2$	V_{CC} = 5 V	0.24	0.34	0.44	V
Pull-up resistance	$R_{U(N1)}$		45	63	85	kΩ
[N2 Pin]						
Input high-level voltage	$V_{IH(N2)}$		4.0		V_{CC}	V
Input low-level voltage	$V_{IL(N2)}$		0		1.5	V
Hysteresis	$\Delta V_{IN(N2)}1$		0.35	0.45	0.55	V
	$\Delta V_{IN(N2)}2$	V_{CC} = 5 V	0.24	0.34	0.44	V
Pull-up resistance	$R_{U(N2)}$		45	63	85	kΩ
[Low Voltage Protection]						
Operating voltage	V_{SDL}			3.75		V
Release voltage	V_{SDH}			4.0		V
Hysteresis	ΔV_{SD}		0.15	0.25	0.35	V

Note: * Design target value. These items are not tested.

Speed Discriminator Counts

N1	N2	Number of counts
High or open	High or open	64
High or open	L	256
L	High or open	128
L	L	512

Three-Phase Logic Truth Table (A high (H) input is the state where $IN^+ > IN^-$.)

Item	F / R = L			F / R = H			Output	
	IN1	IN2	IN3	IN1	IN2	IN3	Source	Sink
1	H	L	H	L	H	L	VH	UL
2	H	L	L	L	H	H	WH	UL
3	H	H	L	L	L	H	WH	VL
4	L	H	L	H	L	H	UH	VL
5	L	H	H	H	L	L	UH	WL
6	L	L	H	H	H	L	VH	WL

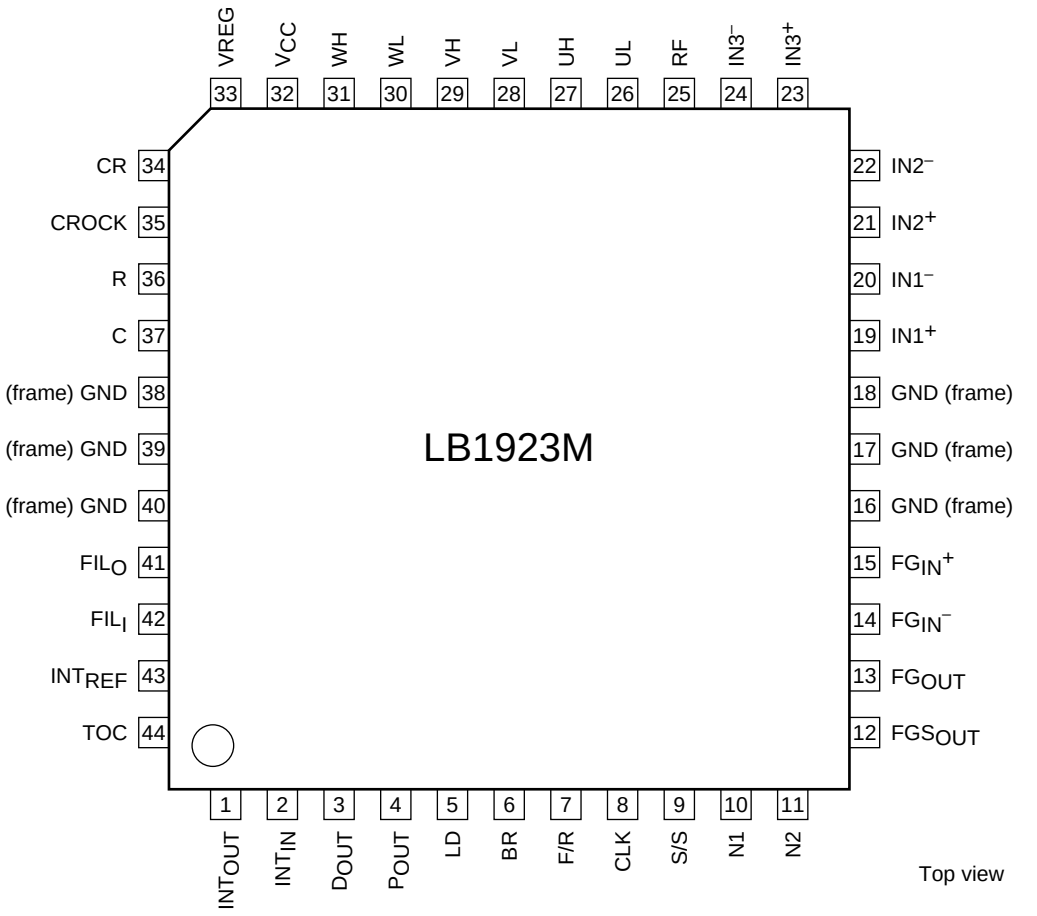
S/S Pin

High or open	Stop
L	Start

BRK Pin

High or open	Brake
L	Released

Pin Assignment



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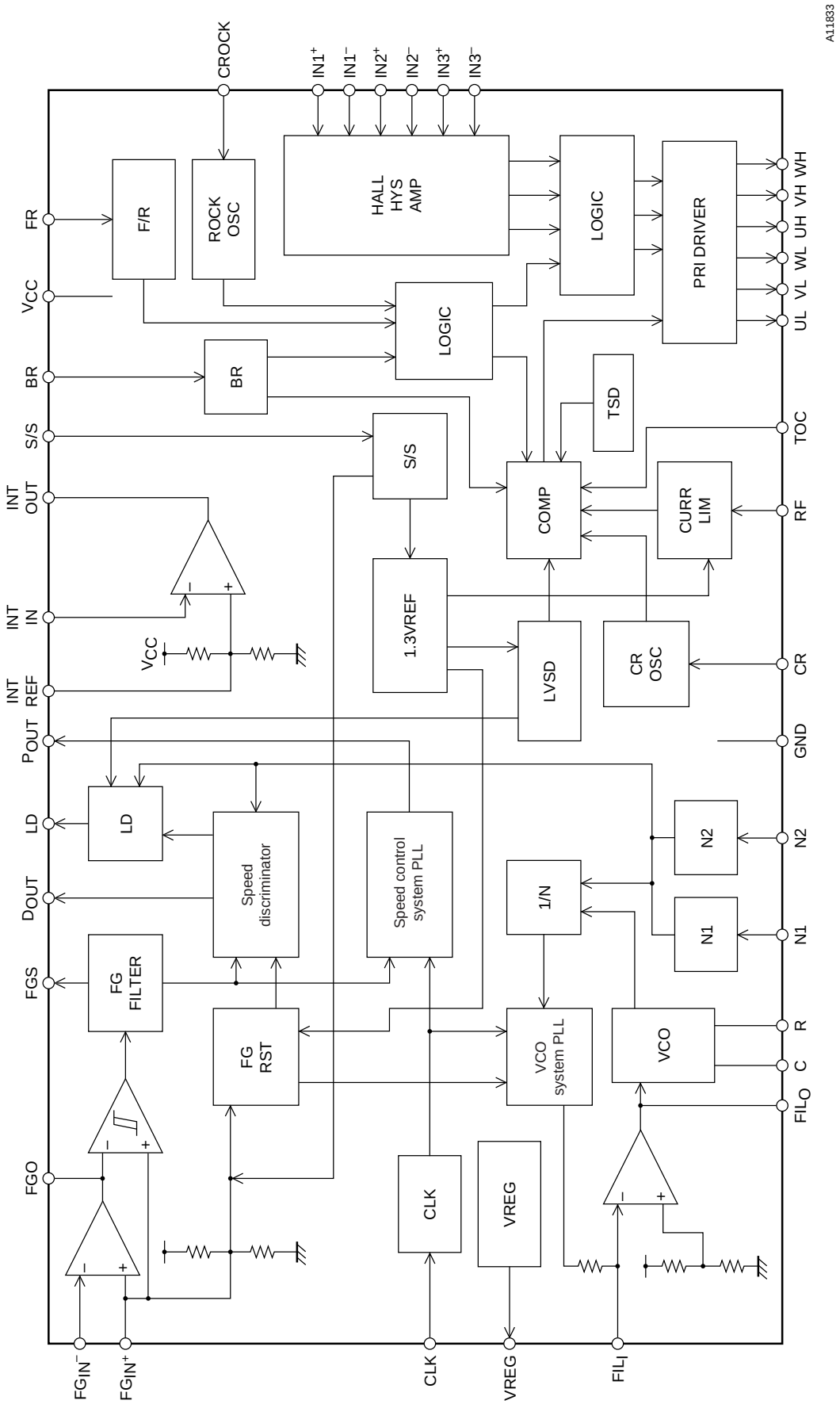
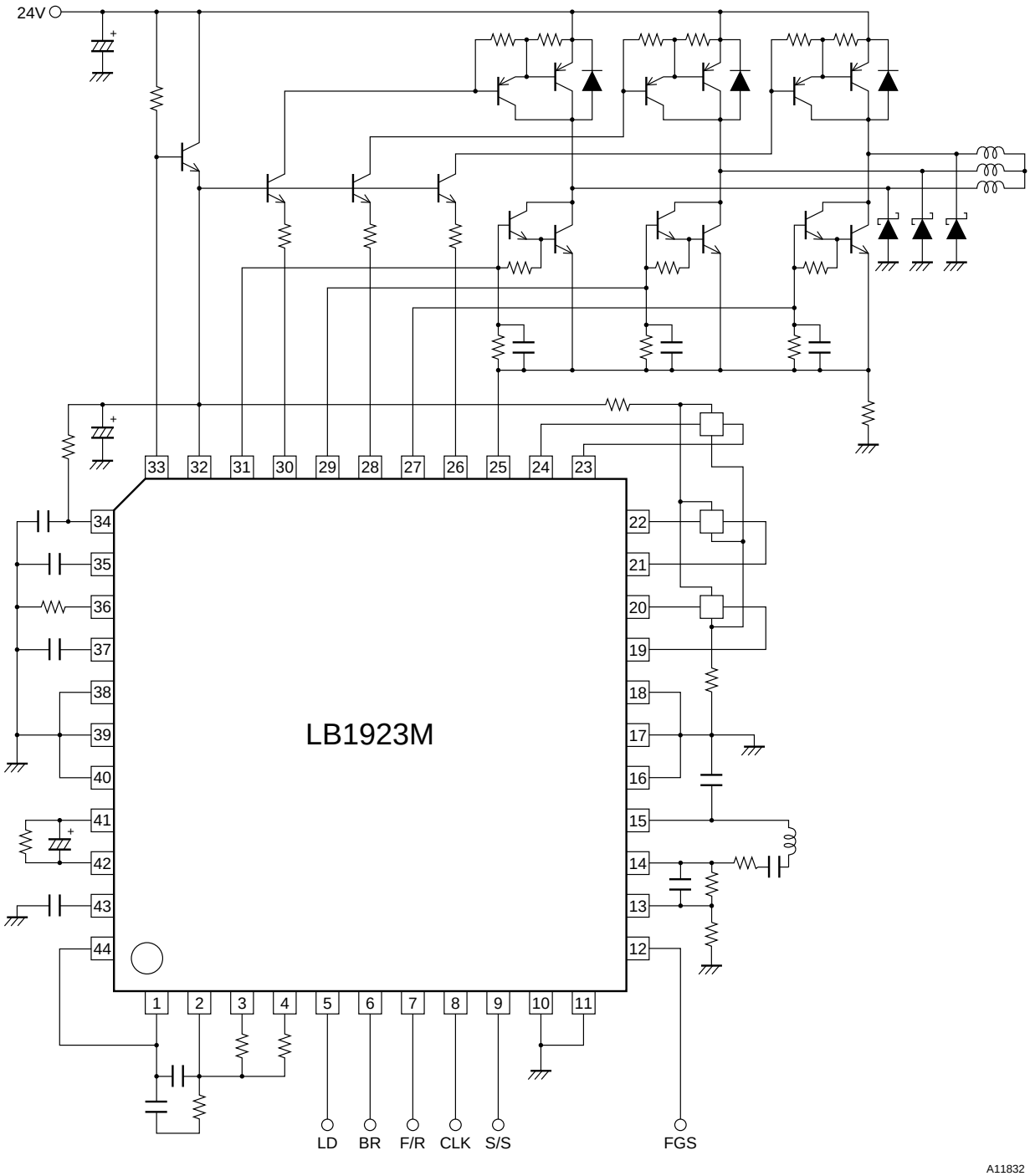
Pin Functions

Pin	Pin No.	Function
$IN1^+$, $IN1^-$ $IN2^+$, $IN2^-$ $IN3^+$, $IN3^-$	19, 20 21, 22 23, 24	Hall inputs for the phases The logic high level corresponds to the state $V_{IN}{}^+ > V_{IN}{}^-$.
UH VH WH	27 29 31	Outputs. These are fixed-current source outputs.
UL VL WL	26 28 30	The duty is controlled by the output pin PWM. These are open collector sink outputs.
V_{CC}	32	A capacitor must be inserted between this pin and ground to prevent noise entering the circuit.
V_{REG}	33	7-V shunt regulator output
GND	16 to 18 38 to 40	Ground
CR	34	Used to set the PWM circuit oscillator frequency.
CROCK	35	Motor lock protection circuit. Reference signal oscillator connection. Used by the circuit that prevents incorrect operation if the clock line is disconnected. A capacitor must be inserted between this pin and ground.
R	36	VCO circuit. This pin sets the charge and discharge current. A resistor must be inserted between this pin and ground.
C	37	VCO oscillator connection. A capacitor must be inserted between this pin and ground. Select a value for that capacitor such that the C pin oscillator frequency does not exceed 1 MHz.
FIL_I	42	Inverting input to the VCO filter amplifier. This pin is connected to the VCO PLL through an (IC internal) 10-kW resistor.
FIL_O	41	VCO filter amplifier output. This pin is connected to the VCO circuit internally.
D_{OUT}	3	Speed discriminator output. A low level is output when the motor is over speed.
R_{OUT}	4	PLL circuit output. Outputs the result of the phase comparison between 1/2fCLK and 1/2fFG.
LD	5	Lock detection output. This is an open collector output. This pin outputs a low level when the motor speed is within the locked range (±6.25%).
INT_{REF}	43	Integrating amplifier noninverting input (the 1/2 V_{CC} potential)
INT_{IN}	2	Integrating amplifier inverting input
INT_{OUT}	1	Integrating amplifier output
TOC	44	Torque command input. Normally, this pin is connected to the INTOUT pin. Lowering the TOC pin potential increases the torque by changing the PWM signal duty for the UL, VL, and WL outputs.
$FGIN^+$	15	FG amplifier noninverting input (the 1/2 V_{CC} potential). A capacitor must be inserted between this pin and ground.
$FGIN^-$	14	FG amplifier inverting input
FG_{OUT}	13	FG amplifier output
FGS_{OUT}	12	FG amplifier (post-Schmitt) output. This is an open collector output.
RF	25	Output current detection. A resistor must be inserted between this pin and ground. This resistor sets the maximum output current I_{OUT} to be 0.5/Rf.
S/S	9	Start/stop control input. Apply a low level for start, and either a high level or an open (high-impedance) state for start.
F/R	7	Forward/reverse control input. Apply a low level for forward, and either a high level or an open (high-impedance) state for reverse.
BR	6	Braking control input (short braking operation). Apply a low level for start, and either a high level or an open (high-impedance) state to brake the motor.
CLK	8	External clock signal input. 10 kHz max.
N1 N2	10 11	Speed discriminator count value selection inputs

Internal Equivalent Circuit Block Diagram



Sample Application Circuit



IC Operation Description

1. Speed Control Circuit

   This IC implements speed control using the combination of a speed discriminator circuit and a PLL circuit. The speed discriminator and the PLL circuit output (using a charge pump technique) an error signal once every two FG periods. As compared to the earlier technique in which only a speed discriminator circuit was used, the combination of a speed discriminator and a PLL circuit allows variations in motor speed to be better suppressed when a motor that has large load variations is used. The FG servo frequency is controlled to be the same frequency as the clock signal input to the CLK pin. This means that the motor speed can be changed by changing the clock frequency.

2. VCO Circuit

   The LB1821M includes an on-chip VCO circuit to generate the reference signal for the speed discriminator circuit. The reference signal frequency is determined by the following formula.

   $f_{VCO} = f_{CLK} \times$ number of counts

   f_{VCO}: Reference signal frequency

   f_{CLK}: Frequency of the externally input clock signal

   The range over which the reference signal can be varied is determined by the resistor and capacitor connected to the R pin (pin 36) and the C pin (pin 37) and by the VCO loop filter constants (the external constants connected to pins 41 and 42).

   (Reference Values)

Supply voltage	R (kΩ)	C (pF)
V_{CC} = 5 V	4.7	390
V_{CC} = 6.3 V	4.7	820

   The value of R must not be less than 2.7 kΩ.

   Applications can handle a wider range of speed variations than would be possible if a fixed number of counts was used by changing the number of discriminator counts (which is related to the divisor in the VCO circuit). The number of counts can be switched between 64, 128, 256, and 512 by setting the N1 (pin 10) and N2 (pin 11) pins.

3. Output Drive Circuit

   To reduce power loss in the output, this IC adopts the direct PWM drive technique. The output transistors (which are external to the IC) are always saturated when on, and the motor drive output is adjusted by changing the duty with which the output is on. Since the (external) output switching is handled by the upper side output transistors, a Schottky diode or similar device must be connected between the output (OUT) and ground. This is because a through current will flows at the instant the upper side output transistors turn on if a diode with a short reverse recovery time is not used. A rectifying diode can be used between OUT and V_{CC}. Transistors that have no parasitic diodes must be used for the lower side output transistors. If these transistors have parasitic diode components, then through currents will occur due to the reverse recovery time of the parasitic diodes despite the inclusion of the external Schottky diodes.

4. Current Limiter Circuit

   The current limiter circuit limits the (peak) current at the value $I = V_{RF}/R_f$ (V_{RF} = 0.52 V (typical), R_f: current detection resistor). The current limitation operation consists of reducing the output duty to suppress the current.

5. Speed Lock Range

   The speed lock range is ±6.25% of the fixed speed. When the motor speed is in the lock range, the LD pin (an open collector output) goes low. If the motor speed goes out of the lock range, the motor on duty is adjusted according to the speed error to control the motor speed to be within the lock range.

6. Notes on the PWM Frequency

   The PWM frequency is determined by the resistor and capacitor connected to the CR pin.

   $f_{PWM} \approx 1/(0.48 \times C \times R)$

   A PWM frequency of between 15 and 25 kHz is desirable. If the PWM frequency is too low, the motor may resonate at the PWM frequency during motor control, and if that frequency is in the audible range, that resonation may result in audible noise. If the PWM frequency is too high, the output transistor switching loss will increase. The external resistor must not have a value under 30 kΩ.

7. Hall Input Signals

   Input signals with an amplitude greater than the hysteresis (60 mV, maximum) are required for the Hall inputs. An input amplitude of 100 mV or greater is desirable, taking noise and other considerations into account. The Hall input DC voltage must be set to fall within the common-mode input voltage range specifications.

8. Forward/Reverse (F/R) Switching

   The F/R pin can be used to switch the motor direction. The direction can be switched with the F/R pin even if the motor is turning. The IC circuit is designed to compensate for the through currents that occur when the direction is switched. However, caution is required with respect to increases in the V_{CC} voltage (due to motor current returning to the power system instantaneously) during direction switching. If this is a problem, try increasing the capacitance of the capacitor connected between the power supply and ground.

9. Brake Switching

   The LB1923M implements a short braking technique in which the upper side transistors (the external transistors) for all phases are turned on. (The lower side transistors for all phases are turned off.) This means that the output current during braking does not pass through the R_f (the current detection resistor) and therefore that the current limiter does not function. Thus caution is required. During braking, the upper side transistors operate at a 100% duty, regardless of the motor speed. The braking function can be operated and released in the start state. Thus motor start and stop control can be performed from the brake pin with the S/S pin at the low level, i.e., with the system in the start state. If the startup time is a problem, the motor can be started with a shorter startup time by using the brake pin for motor start/stop control than it can with the S/S pin. (This is because the stop state is a power saving state, and restarting from this state requires waiting the time required for the VCO circuit to stabilize.)

10. Constraint Protection Circuit

    The LB1923M includes an on-chip constraint protection circuit to protect the IC and the motor in motor constraint mode. If the LD output remains high (indicating the locked state) for a fixed period in the start state, the upper side (external) transistors are turned off. This time is set by the capacitance of the capacitor attached to the CROCK pin. A time of a few seconds can be set with a capacitance of under 0.1 μF.

    $<\text{Set time (s)}> \approx 44 \times C\ (\mu F)$

    To release the constraint protection state, the LB1923M must be set to either the stop state or the brake state, or power must be reapplied. The CROCK pin must be connected to ground if the constraint protection circuit is not used. However, note that the clock disconnection protection circuit described later cannot be used in this case.

11. Clock Disconnection Protection Circuit

    If clock input stops with the LB1923M in the start state, this protection circuit operates and turns off the (external) upper side output transistors. If the clock is reapplied, the IC resumes operation.

12. Low-Voltage Protection Circuit

    The LB1923M includes a low-voltage protection circuit to protect against incorrect operation when power is first applied or if the power-supply voltage (V_{CC}) falls. The (external) upper side output transistors are turned off if V_{CC} falls under about 3.75 volts, and this function is cleared at about 4.0 volts.

13. Power Supply Stabilization

    Since this IC is used in applications that draw large output currents, the power-supply line is subject to fluctuations. Therefore, capacitors with capacitances adequate to stabilize the power-supply voltage must be connected between the V_{CC} pin and ground. If diodes are inserted in the power-supply line to prevent IC destruction due to reverse power supply connection, since this makes the power-supply voltage even more subject to fluctuations, even larger capacitors will be required.

14. Ground Lines

    The signal system ground and the output system ground must be separated and a single ground point must be taken at the connector. Since the output system ground carries large currents, this ground line must be made as short as possible.

    Output system ground ... Ground for R_f and the output diodes

    Signal system ground ... Ground for the IC and the IC external components

15. V_{REG} Pin

If a motor drive system is formed from a single power supply, the V_{REG} pin (pin 33) can be used to create the power-supply voltage (about 6.3 V) for this IC. The V_{REG} pin is a shunt regulator and generates a voltage of about 7 volts by passing a current through an external resistor. A stable voltage can be generated by setting the current to value in the range 1 to 7 mA. The external transistors must have current capacities of at least 80 mA (to cover the I_{CC} + Hall bias current + output current <source> requirements) and they must have voltage handling capacities in excess of the motor power-supply voltage. Since the heat generated by these transistor may be a problem, heat sinks may be required depending on the packages used. If the IC power-supply voltage (4.4 to 7.0 V) is provided from an external circuit, apply that voltage directly to the V_{CC} pin(pin 32). In that case, the V_{REG} pin must either be left open or connected to ground.

16. FG Amplifier

Normally, the FG amplifier is used to construct a filter amplifier such as that shown in the application circuit to reject noise. Since a Schmitt comparator is connected after the FG amplifier, applications must set the amplification so that the amplifier output amplitude is at least 250 mV p-p. (However, a setting that results in an amplitude of 1 to 3 V p-p during steady-state rotation is desirable.) The capacitor connected between the FG_{IN}+ pin (pin 15) and ground is required for bias voltage stabilization and to generate the initial reset pulse for the internal logic. The reset pulse is generated in the time it takes for the FG_{IN}+ pin to go from 0 to about 1.3 V.

17. Integrating Amplifier

The integrating amplifier integrates the speed error pulses and the phase error pulses and converts them to a speed command voltage. At the same time it also sets the control loop gain and frequency characteristics using external components. The integrating amplifier output (pin 1) is normally connected to the TOC pin (pin 44) by an external line. Separating the integrating amplifier output and the PWM control circuit allows applications to switch the integrating amplifier constants using an external operational amplifier, analog switch, or other circuit. This is useful in applications that require integration constant switching due to a wide range of variability in the motor speeds that must be provided.

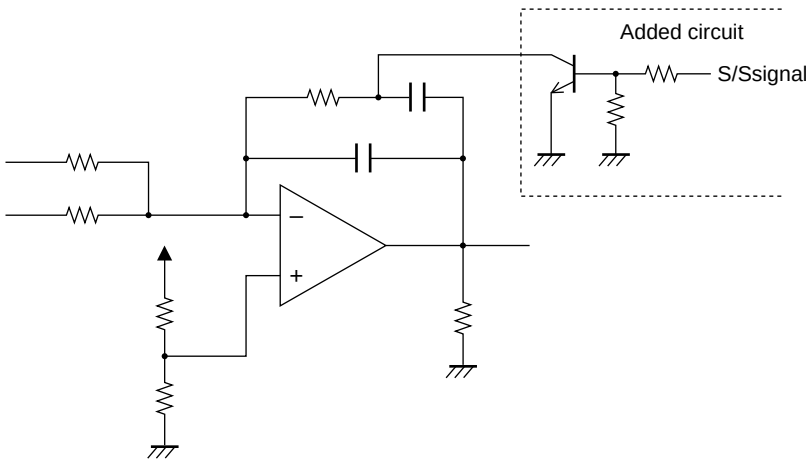
18. VCO Filter Amplifier

The VCO filter amplifier converts the VCO system PLL output to the VCO voltage. The amplifier input resistor (about 10 kΩ) is built in. Therefore, the gain and the frequency characteristics are set by the feedback resistor and the feedback capacitor. Since the range of frequency variation supported becomes narrower as the gain is reduced, it is desirable to set the gain of this amplifier to be 1 or higher.

19. Startup Techniques

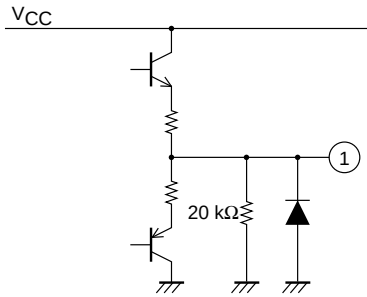
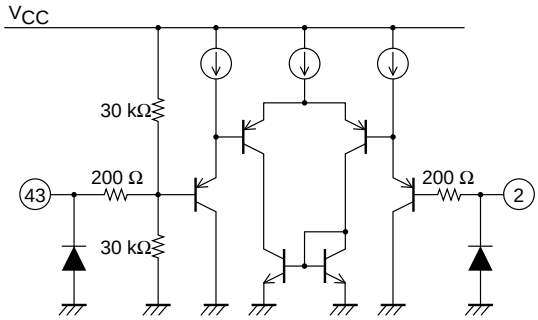
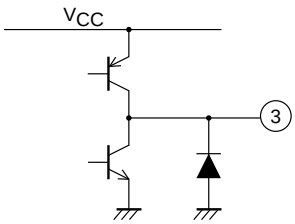
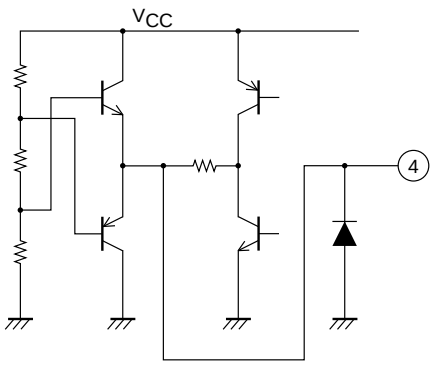
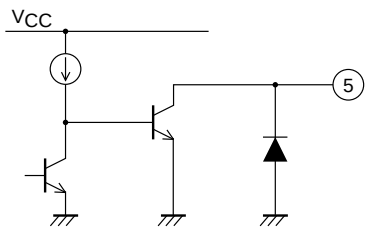
If the motor is started and stopped repeatedly over a short period, the charge accumulated on the integrating amplifier's external capacitor may become a problem. (This can result in abnormal speed overshooting at startup and other problems.) The circuit shown below can be effective at resolving this problem.

Integrating amplifier related external circuit



A11834

Pin Functions

Pin No.	Pin	Functions	Equivalent circuit
1	INT_{OUT}	Integrating amplifier output (speed control)	
2	INT_{IN}	Integrating amplifier inverting input	
43	INTREF	Integrating amplifier noninverting input (a potential of 1/2 V_{CC})	
3	D_{OUT}	Speed discriminator output Acceleration → high, deceleration → low	
4	P_{OUT}	Speed control system PLL output Outputs the phase comparison result for 1/2 f_{CLK} and 1/2 f_{FG}.	
5	LD	Speed lock detection output Goes low when the motor speed is within the speed lock range (±6.25%).	

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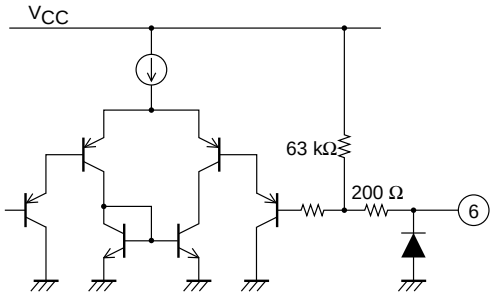
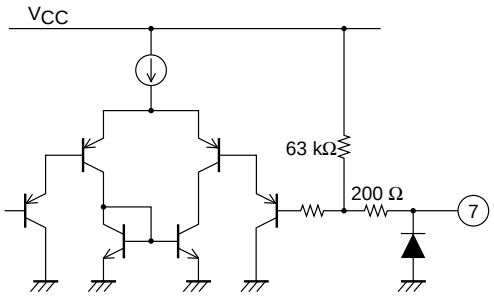
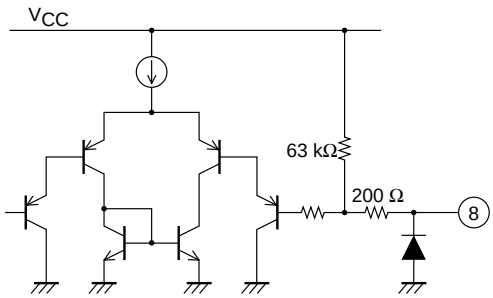
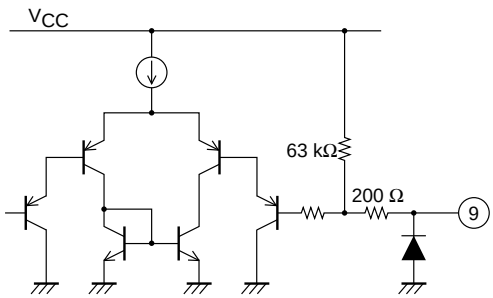
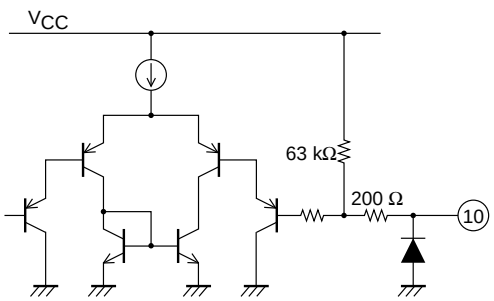
Pin No.	Pin	Functions	Equivalent circuit
6	BR	Brake control (short braking operation) Low: 0 to 1.5 V High: 4.0 V to V_{CC} Goes high when left open. High or open for brake mode operation. The hysteresis is about 0.45 V.	
7	F/R	Forward/reverse control Low: 0 to 1.5 V High: 4.0 V to V_{CC} An open state functions as a high-level input. Low for forward. The hysteresis is about 0.45 V.	
8	CLK	External clock signal input Low: 0 to 1.5 V High: 4.0 V to V_{CC} An open state functions as a high-level input. The hysteresis is about 0.45 V. f = 10 kHz, maximum	
9	S/S	Start/stop control Low: 0 to 1.5 V High: 4.0 V to V_{REG} An open state functions as a high-level input. Low for start. The hysteresis is about 0.45 V.	
10	N1	Speed discriminator count switching Low: 0 to 1.5 V High: 4.0 V to V_{CC} An open state functions as a high-level input. The hysteresis is about 0.45 V.	

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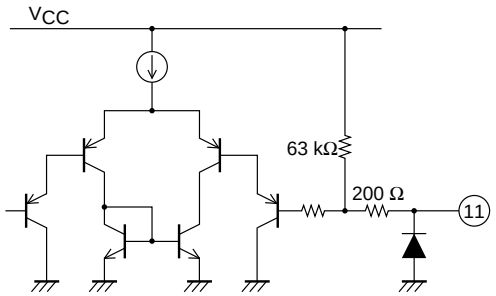
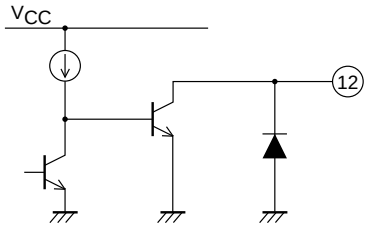
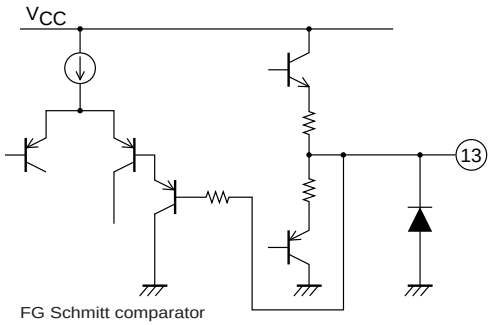
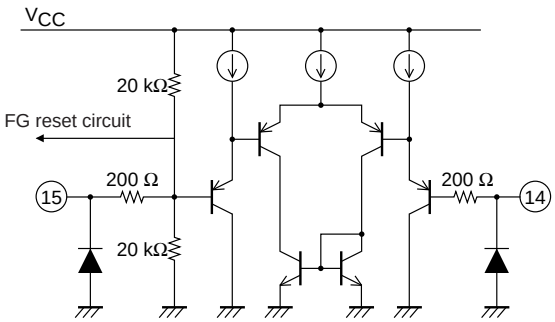
Pin No.	Pin	Functions	Equivalent circuit
11	N2	Speed discriminator count switching Low: 0 to 1.5 V High: 4.0 V to V_{CC} An open state functions as a high-level input. The hysteresis is about 0.45 V.	
12	FGS_{OUT}	FG amplifier output (after the Schmitt circuit) This is an open collector output.	
13	FG_{OUT}	FG amplifier output This pin is connected to the FG Schmitt comparator circuit internally in the IC.	
14 15	FG_{IN}– FG_{IN}+	FG amplifier inputs An initial reset is applied to the logic circuit block by connecting a capacitor (of about 0.1 μF) between the FGIN+ pin and ground.	
16 to 18 38 to 40	GND	Ground connections These pins are all connected internally to the frame.	

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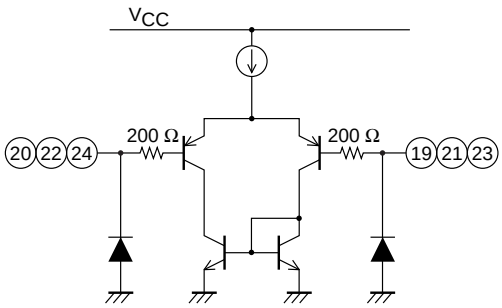
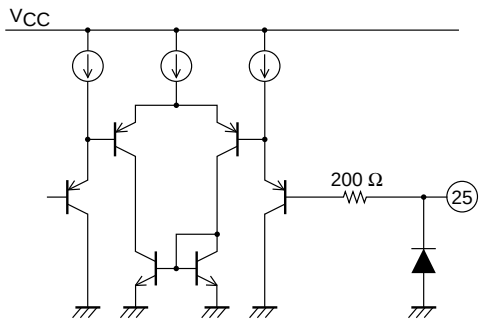
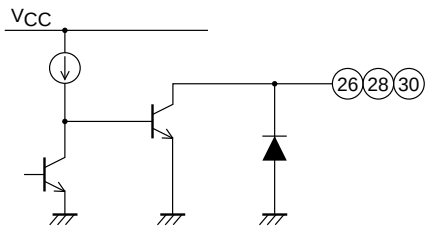
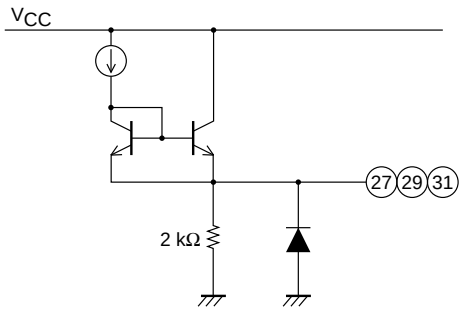
Pin No.	Pin	Functions	Equivalent circuit
19 20 21 22 23 24	$IN1^+$ $IN1^-$ $IN2^+$ $IN2^-$ $IN3^+$ $IN3^-$	Hall inputs High is defined as $IN^+ > IN^-$, and low as the opposite. An amplitude of 100 mV p-p (differential) or more is desirable in the Hall signals. Connect capacitors between the IN^+ and IN^- pins if noise on the Hall signals causes problems.	
25	RF	Output current detection Connect a resistor between this pin and ground. The output limitation maximum current, I_{OUT}, is set to be $0.52/R_f$ by this resistor.	
26 28 30	UL VL WL	This IC implements duty control using output signal PWM. These are open collector sink outputs.	
27 29 31	UH VH WH	Outputs (Fixed current source outputs)	
32	V_{CC}	Power-supply voltage Connect a capacitor between this pin and ground for power supply stabilization.	

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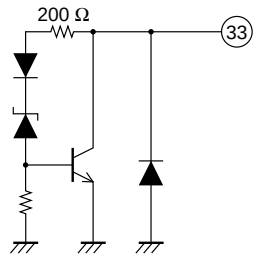
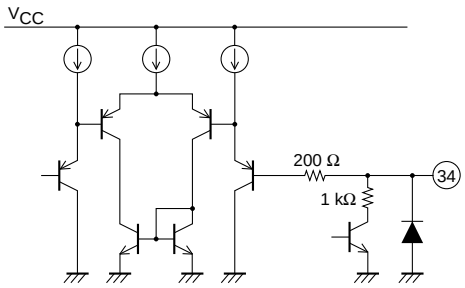
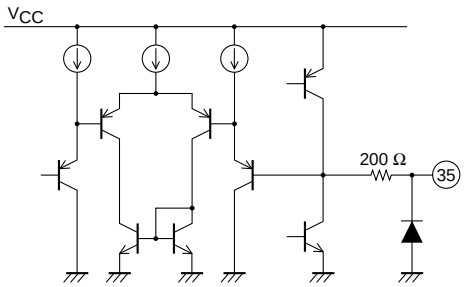
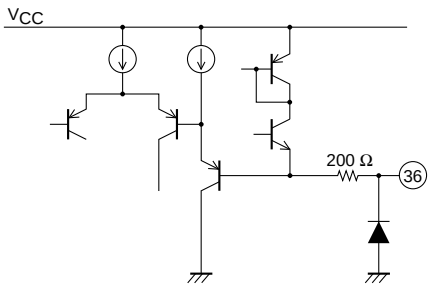
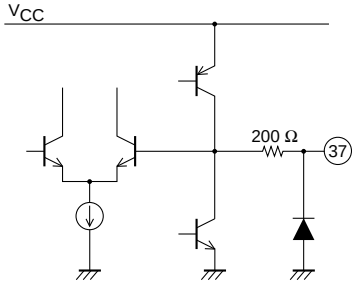
Pin No.	Pin	Functions	Equivalent circuit
33	V_{REG}	7-V shunt regulator output	
34	CR	PWM oscillator frequency setting	
35	CROCK	Sets the operating time for the lock protection circuit. A protection operating time of about 2.1 seconds can be set by connecting a capacitor (of about 0.047 µF) between this pin and ground.	
36	R	Setting for the charge current used for the VCO circuit C pin Connect a resistor between this pin and ground. The value of that resistor must not be lower than 2.7 kΩ.	
37	C	VCO oscillator connection. This pin sets the VCO frequency. Connect a capacitor between this pin and ground. Set the value of the capacitor so that the oscillator frequency does not exceed 1 MHz.	

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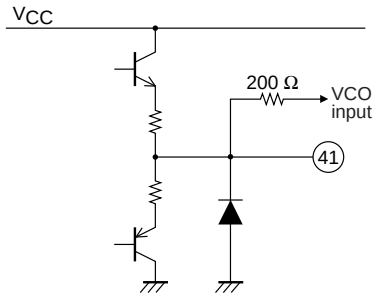
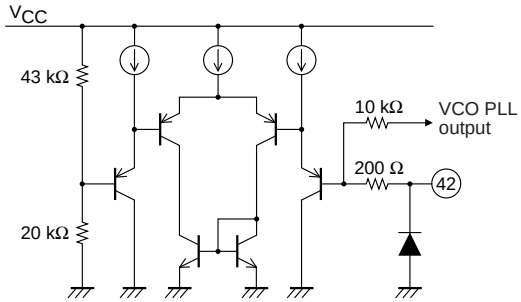
Pin No.	Pin	Functions	Equivalent circuit
41	FIL_O	VCO filter amplifier output This pin is connected to the VCO circuit internally in the IC.	
42	FIL_I	VCO filter amplifier inverting input This pin is connected through a 10-kΩ resistor internally in the IC to the VCO system PLL output.	
44	TOC	Torque command input This pin is normally connected to the $INT_{.OUT}$ pin. When the TOC voltage falls, the PWM duty is increased. Do not apply a voltage in excess of V_{CC} - 0.5 V. (An input from a normal operational amplifier is desirable.)